



VK1640

8x16 LED Driver

Dedicated circuit for LED driver control

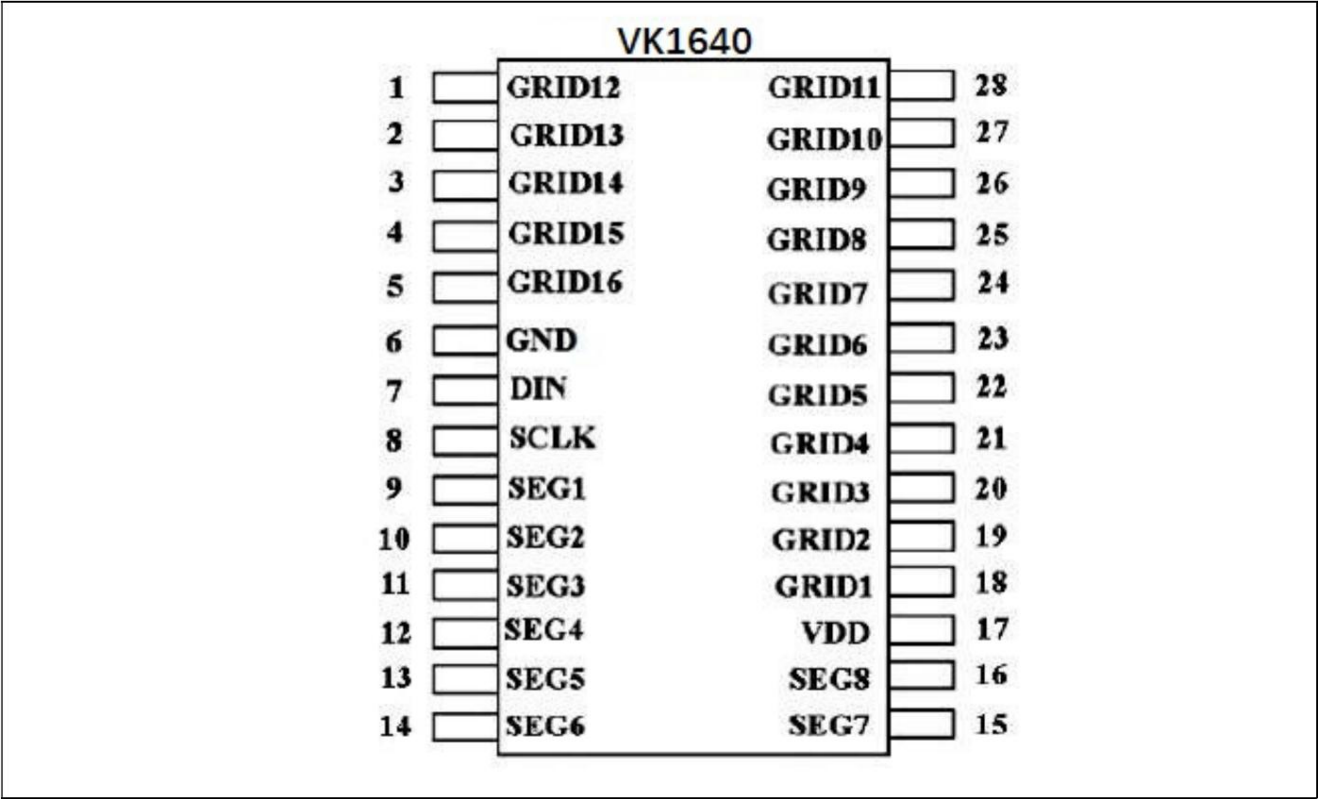
Overview

The VK1640 is a dedicated circuit for driving and controlling LEDs (Light Emitting Diode Displays), integrating an MCU digital interface. Data latch and LED high-voltage driver. This product uses CMOS technology and is mainly used in driving small LED displays.

Features

- Fabricated using CMOS technology
- Display mode (8 segments × 16 bits)
- Brightness adjustment circuit (8-level adjustable duty cycle)
- Two-wire serial interface
- Oscillation method:
 - Built-in RC oscillator
 - Built-in power-on reset
 - SOP28 package

Pin arrangement diagram





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Pin Description

symbol	Pin Name	pin number	illustrate
FROM	Data Input	7	Serial data input
SCLK	Clock Input	8	Input data on the rising edge
SEG1~SEG8	Output (Segment)	9-16	Segment output, P-tube open drain
GRID1~GRID11 GRID12~GRID16	Output (bits)	18-18 1-5	Bit output, N-channel open-drain transistor
VDD	Logic power supply	17	5V±10% connected
GND	and logic ground	6	to system ground

Electrical parameters

symbol	Parameter name	condition	numerical values	unit
VDD	Logic power supply voltage		4.5~6.0	In
Ios	SEG drive output current	VDD=5V, Ta=25°C	-50	m.a.
Yog	GRID drive output current VDD=5V, Ta=25°C		200	m.a.
PD	Power loss		400	mW
Tj	Operating temperature		-40~80	°C
Ts	Storage temperature		-65~150	°C

Normal operating range (Ta = -40 ~ +80°C, GND = 0V)

symbol		Minimum	Typical	Maximum	Unit
VDD	Parameter logic		5		In
HIV	power supply voltage	0.7VDD			VDD In
WILL	high level input voltage low level input voltage	0		0.3VDD V	

Electrical characteristics (unless otherwise specified, Ta = -20°C~70°C, VDD = 3V~3.6V, GND=0V)

symbol	Parameter name	Test conditions	Minimum	Typical	Maximum	Unit
Iseg	High-level output current	VDD=3.3V VO=VDD-2V	-32	-34	-38	m.a.
Igrid		VDD=3.3V VO=VDD-2V	-25	-30	-44	m.a.
Iout	Low-level output current	Vo=VDD-3V	80	140		m.a.
I	Low-level output current	Vo=VDD-3V	4			m.a.
RL	Output pull-down resistor			10		KΩ
Iin	Input current	VI=VDD/GND			±1	a



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HIV	High-level input voltage CLK, DIN, STB 0.7VDD					In
Will	Low-level input voltages CLK, DIN, STB				0.3VDD V	
Vh	Lag voltage	CLK, DIN, STB		0.35		In
IDDdyn Dynamic Current Loss		No load, display off			100	a

Switching characteristics (unless otherwise specified, Ta = -20°C~70°C, VDD = 4.5V~5.5V)

Parameter name symbol	Test conditions	Minimum	Typical	Maximum	Unit
Oscillation frequency Fosc	R=16.5K		500		KHz
Transmission delay time	T PLZ			300	ns
	T PZL			100	ns
Ascent Time	T 1TZH			2	us
	T 2TZH			0.5	us
Descent time T TZH	CL=300pF, SEGn~GRIDn			120	us
Maximum clock frequency Fmax	50% duty cycle	1			MHz
Input capacitor	C			15	pF

Timing characteristics (unless otherwise specified, Ta = -20°C~70°C, VDD = 4.5V~5.5V)

symbol	Parameter name	Test conditions	numerical values	unit
PWCLK	Clock pulse width		400	us
PESTB	strobe pulse width		1	us
T setup	Data creation time		100	ns
T hold	Data retention time		100	ns
T wait	Waiting time	SCLK~SCLK	1	us

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The address command

setting instruction is used to configure data write and read operations. Bits B1 and B0 cannot be set to 01 or 11.

MSB

LSB

B7 B6 B5 B4 B3 B2 B1 B0								Function	illustrate
0	1	irrelevant items Fill in 0			0		0	Data read/write mode settings	Write data to register
0	1			0				Address addition mode settings	Automatic address increment
0	1			1					Fixed address
0	1		0					Internal test mode settings	Normal mode
0	1		1						Test mode

Data command settings

B7	B6	B5	B4	B3	B2	B1	B0	Display address
1	1	Enter 0 for irrelevant items.		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05:00
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H
1	1			1	0	0	0	08H
1	1			1	0	0	1	09H
1	1			1	0	1	0	0AH
1	1			1	0	1	1	0BH
1	1			1	1	0	0	0CH
1	1			1	1	0	1	0DH
1	1			1	1	1	0	0EH
1	1			1	1	1	1	0FH

This instruction is used to set the address of

the display register. If the address is set to 10H or higher, the data is ignored until a valid address is set. At power-on, the address defaults to 00H.



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Display control

MSB				LSB				Function	illustrate
B7 B6 B5 B4 B3 B2 B1 B0									
1	0	irrelevant items Fill in 0				0	0	0	Set pulse width 1/16 Set pulse width
1	0					0	0	1	2/16 Set pulse width 4/16 Set pulse
1	0					0	1	0	width 10/16 Set pulse width 11/16 Set
1	0					0	1	1	pulse width 12/16 Set pulse width 13/16
									Set pulse width 14/16 Display off
1	0					1	0	1	
1	0					1	1	0	
1	0					1	1	1	
1	0					0			Display switch
1	0					1			set up
									Show open

Interface

Description: The microprocessor communicates with the VK1640 via a two-wire bus interface. When inputting data, DIN is active when SCLK is high. The signals on the DIN pin must remain unchanged; the signals on the DIN pin can only be changed when the clock signal on the SCLK pin is low. Data input is always transmitted with the least significant bit first and the most significant bit last. The condition for starting data input is that SCLK is high and DIN changes from high to low; the condition for ending data input is that SCLK is high and DIN changes from low to high.

The instruction transmission process is as follows:

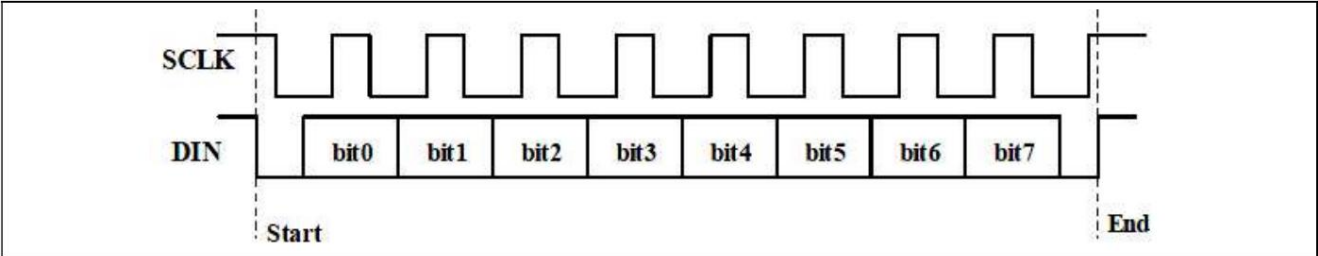


Figure 1 Command Transmission

Automatic data address incrementing mode

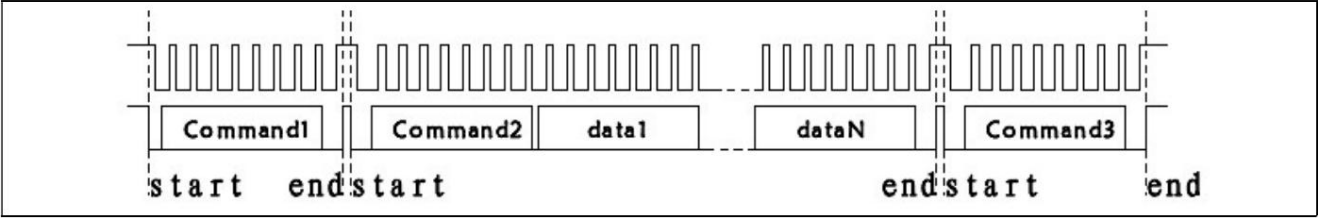


Figure 2 Automatic address write data mode

Command1: Set Data Command

Command2: Set data address

Date1~N: Transmit display data to the address following Command2 (maximum 16 bytes).

Command3: Display control commands



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Fixed address write data mode

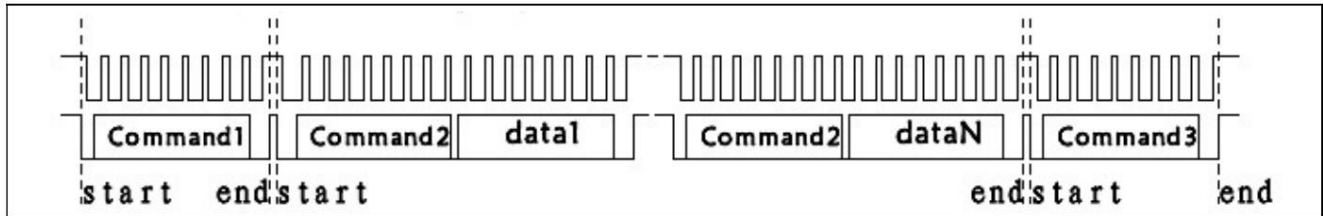


Figure 3 Fixed address write data mode

Command1: Set Data Command

Command2: Set display address

Date1~N: Transmit display data to the address following Command2 (maximum 16 bytes).

Command4: Display control commands

Display cycle

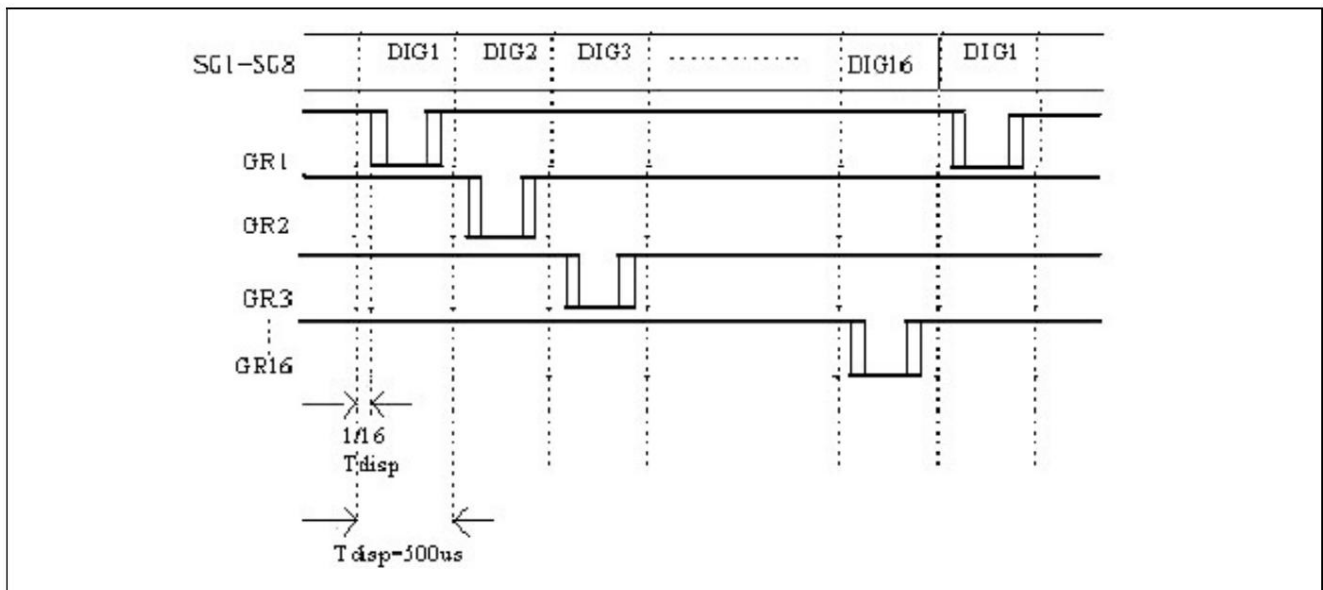


Figure 4 shows the data cycle.



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Application Examples

Common cathode digital tube connection principle

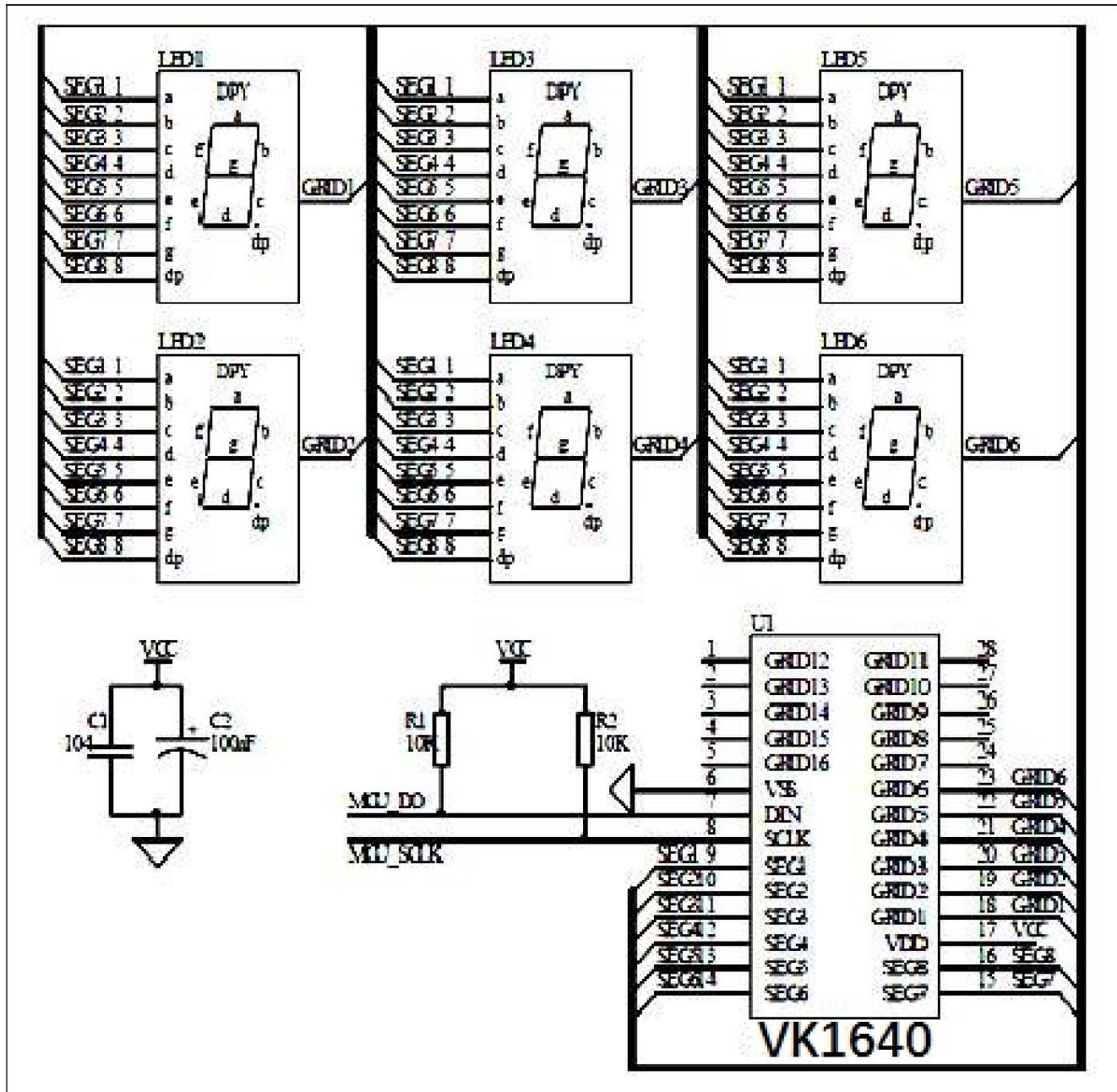


Figure 5. Schematic diagram of VK1640 driving common cathode digital tube.



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Package size

